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Self-Biasing Differential Buffer with Transmission-Gate Bias Generator

Abstract

A self-biasing differential buffer generates a self-bias voltage from its inputs. A first amplifier receives a first input signal on gates of four transistors - p and n-channel drive transistors in a drive branch and p and n-channel bias-generating transistors in a bias-generating branch. Current source and current sink transistors source and sink current to both branches. The drains of the drive transistors drive a differential output, while the drains of the bias-generating transistors drive through a transmission gate to a self-bias node. The second amplifier receives the second input signal and has the same structure, with one branch driving the self-bias voltage through another transmission gate, and another branch driving a complementary differential output. The bias-generating branches use smaller transistors so that only a small current is used to generate the self-bias voltage. The self-bias node is fed to the gates of current source and sink transistors.